MILLIMETER-WAVE PERFORMANCE OF CHIP INTERCONNECTIONS USING WIRE BONDING AND FLIP CHIP

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Abstract - **The performances of two different interconnection techniques for coplanar MMICs, wire bonding and flip chip, are investigated at millimeter-wave frequencies. By developing an accurate model for the interconnections, which is validated with experimental data up to 120 GHz, the limitations with respect to frequency and interconnection distance of either technique are pointed out, yielding useful data for the design of hybrid MMW-subsystems.**

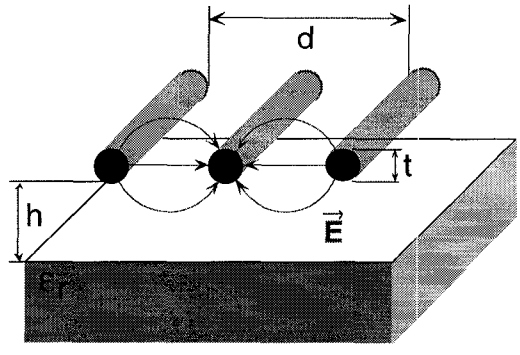

Fig. 1: Raised coplanar waveguide model

I. INTRODUCTION

ALONG with the rapid advances in microwave and millimeter-wave subsystem development throughout the last years, a growing interest concerning chip interconnection techniques has developed, since the quality of these interconnects has a large impact on the performance of the entire subsystem, especially at high frequencies. The use of bond wires is still very widespread, due to the rather simple technology involved. A number of studies concerning the electrical performance of bond wire interconnections have been presented for microstrip [1, 2] and coplanar [3] configurations, indicating a drastic increase of the loss as the frequency or the interconnection distance are increased, which places certain limitations on this technique. Flip chip, though already over thirty years old, was introduced into millimeter-waves only recently, and theoretical investigations have led to very promising results [4]. Because the interconnection distance can be reduced until the proximity of the mounting substrate starts effecting the circuits on the chip [5, 6], very good performance even at frequencies over 100 GHz can be expected. This presentation describes the electrical performances of both techniques, by introducing a suitable model whose validity is confirmed by experimental data at MMW-frequencies and which therefore allows a good estimation of the limitations with respect to the maximum frequency or interconnection distance of either technique.

II. WIRE BONDING

The behavior of bond wire interconnections at millimeter-wave frequencies is determined by the fact that, as frequency is increased, the length of the wires reaches significant fractions of wavelength, and the wires exhibit transmission line properties. In the case of coplanar bond wire interconnections, which consist of three wires to connect the center conductors as well as the ground planes, a suitable model to account for this behavior is the raised coplanar waveguide, that is shown in fig. 1. Here, contrary to the regular CPW, the shapes of the ground and center conductors are given by the cross-section of the bond wires, and the substrate is composed of an air layer of thickness h, which is either grounded by a metallic surface or located on top of a dielectric layer, corresponding to a mounting substrate. The characteristic impedance and the effective permittivity of this transmission line are shown in fig. 2 for

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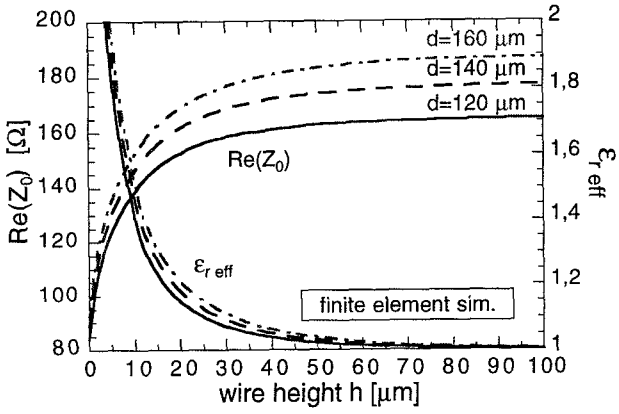

Fig. 2: $Re(Z_0)$ and $\varepsilon_{r\,eff}$ vs. wire height above GaAs substrate ($\varepsilon_r = 12.9$) for raised coplanar waveguide describing a bond interconnection with t = 17 µm gold bond wires.

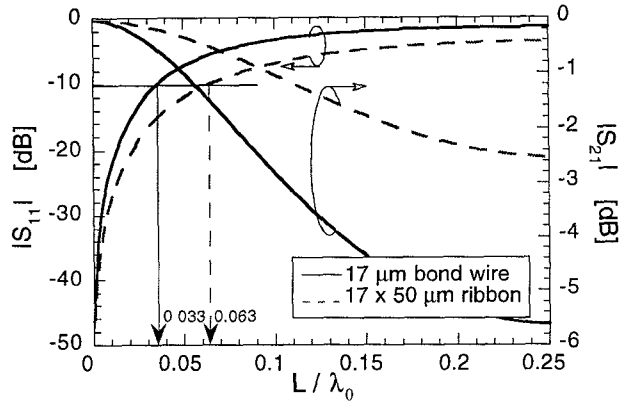

Fig. 4: Simulated return loss and insertion loss of bond wire and bond ribbon interconnection vs. normalized wire length L/λ_0. Maximum lengths for $|S_{11}|$ better than -10 dB.

different ground-wire to ground-wire spacings d, as a function of the wire height h, as they were computed using the electromagnetic field simulator HFSS. Since the height of the wires above the mounting surface is roughly given by the thickness of the chips to be connected, h will in be of the order of 630 µm for coplanar MMICs, along the most part of the wire. In this case, fig. 2 indicates that the characteristic impedance of the corresponding raised CPW is of the order of 170 Ohm, depending on the value of d, while the influence of the mounting substrate on the wavelength is negligible. The exact wire height is not important since beyond 100 µm both parameters are independent of h. At each end, however, the wires run for a short section in close proximity to the chip surface since the bond contacts

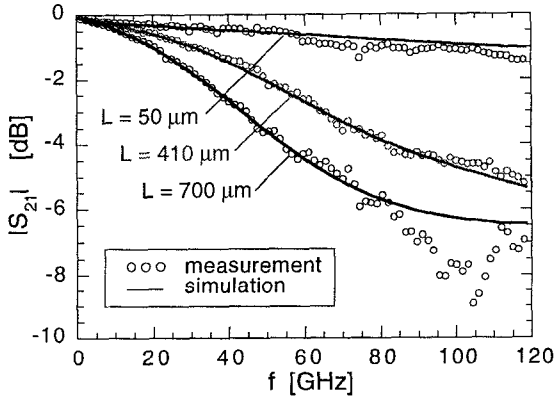

Fig. 3: Measured and simulated insertion loss vs. frequency for bond wire interconnections of different lengths.

are placed not exactly at the chip edge, but typically about 30 µm further inside the chip. These regions have to be treated separately, since there Z_0 is only about 130 Ohm and the effective permittivity is greater than unity. The wire height h, though slightly changing, is approximated by a constant average value, since no further improvement is achieved by accounting for the variations of h within these sections. A sufficient model to describe the entire coplanar bond wire interconnection therefore has to consist of three sections of raised CPW connected in series. Figure 3 shows the measured insertion loss for three bond wire interconnections of different lengths together with the data that was obtained using the raised CPW model, indicating good agreement between experiment and simulation. Only as the wire length reaches about one fourth of the wavelength the model seems to fail because of additional loss due to radiation effects, which are not included in the model. Figure 4 shows the return loss and the insertion loss for interconnections using either 17 µm bond wires or 17 x 50 µm bond ribbons, as a function of the wire length divided by the free space wavelength as they were obtained using the raised CPW model. This graph can be used to determine the maximum interconnection distance at a certain operating frequency, depending on the desired quality of the interconnection. As shown, an interconnection with a return loss better than -10 dB requires bond wires not longer than $0.033 \cdot \lambda_0$, which is only about 100 µm at 94 GHz. If the wire length exceeds this maximum value, due to different substrate thicknesses or other reasons, an interconnection of the same quality can only be achieved at the cost of an additional bond wire compensation.

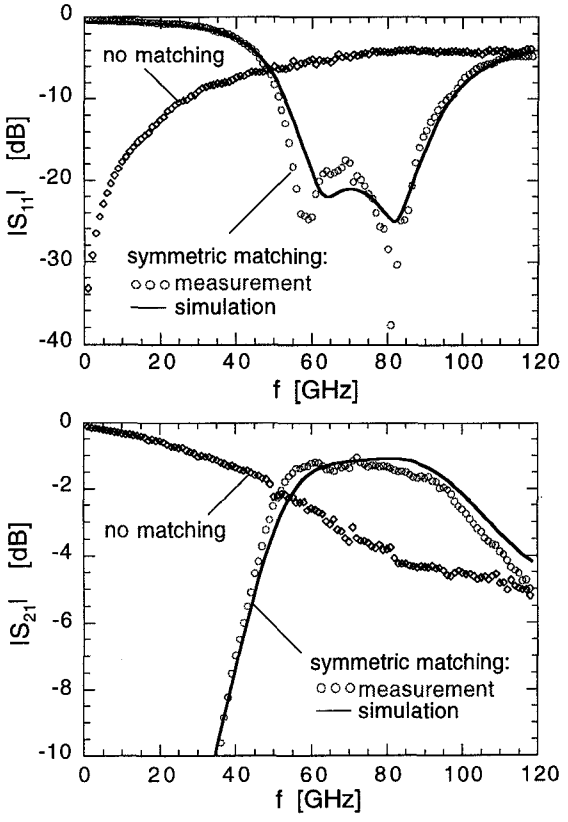

Fig. 5: Return loss and insertion loss of a 410 µm long bond wire interconnection using 17 µm wires with and without symmetric matching.

An example for a compensated bond wire interconnection that has additional matching networks at either end of the wires is shown in fig. 5. An improvement of the performance is achieved over a large bandwidth, compared to the unmatched interconnection. Despite the wire length of 410 µm, the insertion loss and return loss are better than -1.5 dB and -18 dB, respectively, in the frequency range from 55 GHz to 90 GHz. However, this symmetric bond wire compensation demands additional chip area on each MMIC, and results in an output impedance that is different from the usual 50 Ohm reference. Therefore, in many cases an asymmetric compensation on only one side of the interconnection would be preferable, even though the matching is inferior and the bandwidth decreases by about 30 %.

III. FLIP CHIP

The use of coplanar transmission lines for MMICs is the key issue that allows applying flip chip as an alternate interconnection technique for millimeter-wave systems, apart from wire bonding. Since the fields on a coplanar line are well confined to the slots on the top surface of the chip, a good transition from the substrate to the MMIC as well as only a low impact of the mounting substrate on the chip performance are guaranteed. Figure 6 shows the flip chip transition between two CPW lines on dielectric materials, using three metallic bumps to connect the ground and the center conductors. Because the bump height h_b is kept small compared to the length of bond wires, and the bump diameter t_b exceeds that of the bond wire, a considerable improvement of the electrical interconnection properties is achieved. Below we shall investigate the losses of the interconnection and the effect of a metallized substrate surface on the propagation properties of a CPW line located on the MMIC.

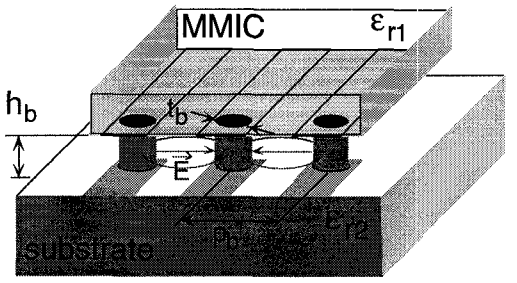

Fig. 6: Flip chip interconnection of coplanar MMIC

To obtain the minimum bump height which still allows proper functioning of the assembled circuit, the transmission line parameters of different CPWs were measured at MMW-frequencies, while a metallic lid representing the substrate surface was positioned at various distances above it. The measured results for the effective permittivity and the characteristic impedance of two coplanar waveguides with ground to ground spacings of 50 µm and 100 µm, as a function of the distance which represents the bump height, are shown in fig. 7. These measurements indicate that the influence of the substrate surface is negligible when the bump height is equal to or greater than the ground to ground spacing of the transmission lines used in the circuit. The results are found to be independent of frequency. Simulations show that the propagation characteristics of the flipped CPW are affected less by a dielectric surface, which means that the minimum bump height h_b can be made smaller than the ground to ground spacing

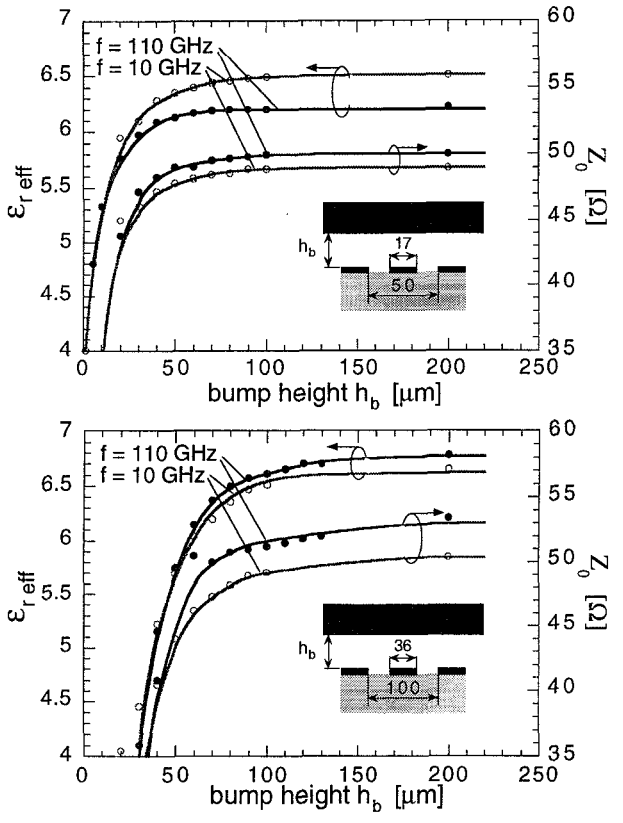

Fig. 7: Measured influence of the mounting substrate on the transmission line parameters of flipped coplanar waveguides on GaAs with ground to ground spacings d = 50 µm and d = 100 µm.

of the CPW.

The losses which occur at flip chip interconnections were found using a raised CPW model corresponding to that for the bond wire. Simulations result in a characteristic impedance of $Z_0 = 109$ Ohm for a bump diameter of $t_b = 40$ µm and a bump pitch of $p_b = 90$ µm. Figure 8 shows the calculated return loss and insertion loss for the single flip chip transition of fig. 6 as a function of the bump height h_b. The comparison with the performance of bond wire interconnections in fig. 4 immediately reveals the electrical superiority of the flip chip technology. Insertion losses below 0.5 dB are achieved even at frequencies beyond 100 GHz, while the return loss indicates that no additional matching is needed. Besides, the flip chip architecture makes the system design much more flexible since the locations for the signal input and output lines are no longer restricted to the chip perimeter as it is the case for wire bonding.

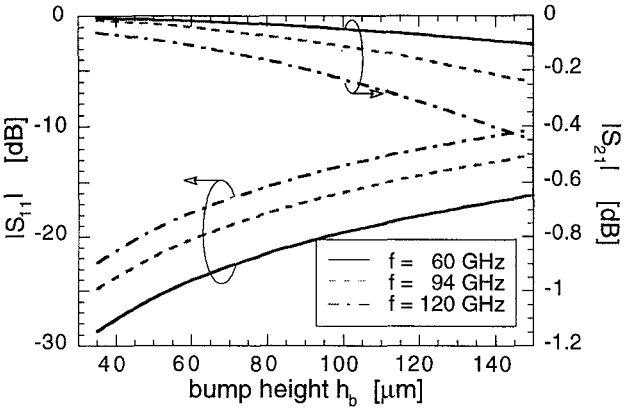

Fig. 8: Simulated return loss and insertion loss of a single flip chip transition using the bump diameter $t_b = 40$ µm and the bump pitch $p_b = 90$ µm as a function of the bump height h_b.

IV. ACKNOWLEDGMENT

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